What is claimed is:

1. A slew rate controlling method for output data comprising:

a step of sampling a potential difference among two or more power supplies with specified timing to generate signals each indicating a tendency in a change in said potential difference and of changing a transition speed occurring at time of a rise or fall of output data based on said signals each indicating a tendency in a change in said potential difference.

2. A slew rate controlling system for output data comprising:

a potential difference detecting means to detect a decrease in a potential difference among a first power supply and a second power supply to produce a first signal with specified timing and to detect an increase in a potential difference between said first power supply and said second power supply to produce a second signal with specified timing; and

a slew rate controlling means to exert, when said first signal is significant, control so as to enlarge a transition speed occurring at time of a fall of output data and, when said second signal is significant, so as to enlarge a transition speed occurring at time of a rise of output data to produce output data.

3. The slew rate controlling system for output data according to Claim 2, wherein said potential difference detecting means comprises a first differential amplification means to produce an output when a potential difference between said first power supply and said second power supply becomes a preset value or less, a first sampling means to latch an output from said first

differential amplification means with specified timing and to produce said first signal, a second differential amplification means to produce an output when a potential difference between said first power supply and said second power supply becomes said preset value or more, and a second sampling means to latch an output from said second differential amplification means and to produce said second signal.

4. The slew rate controlling system for output data according to Claim 2, wherein, in said potential difference detecting means, specified timing with which said first or second signal is produced is timing with which an external command is received.

5. The slew rate controlling system for output data according to Claim 4, wherein said external command is at least one of a writing command and a reading command in a memory device, an active command to provide an instruction for initiating operations of row systems, an MRS (Mode Register Set) command to provide an instruction for setting of an operating mode set register, and an EMRS (Extended Mode Register Set) command to provide an instruction for setting of an extended operating mode set register.

6. The slew rate controlling system according to Claim 2, wherein, in said potential difference detecting means, specified timing with which said first or second signal is produced is timing that is set at an another register when said MRS command to provide an instruction for setting of an operating mode set register or said EMRS command to provide an instruction for setting of an

extended operating mode set register is received.

7. The slew rate controlling system according to Claim 2, wherein said slew rate controlling means comprises a driver means to exert, when said first signal is significant, control on said first and second input data so as to enlarge a transition speed occurring at time of a fall of output data and, when said second signal is significant, so as to enlarge a transition speed occurring at time of a rise of output data and to produce first and second output data and an output buffer means to produce a high-level output when both said first and second output data are at a low level and to produce a low-level output when both said first and second output data are at a high level.

8. The slew rate controlling system according to Claim 7, wherein said slew rate controlling means comprises a logically-operated means having a first logical device to propagate and output a data signal to be output at time of a rise of an external clock when said output buffer is in an enable state and, when said output buffer is in a disenable state, its output is at a high level all the time, a second logical device to propagate and output a data signal to be output at time of a fall of an external clock when said output buffer is in an enable state and, when said output buffer is in a disenable state, its output is at a high level all the time, a third logical device to propagate and output a data signal to be output at time of a rise of an external clock when said output buffer is in an enable state and, when said output buffer is in a disenable state, its output is at a low level all the time, and a fourth logical device to propagate and output a

data signal to be output at time of a fall of an external clock when said output buffer is in an enable state and, when said output buffer is in a disenable state, its output is at a low level all the time and a selector means to select an output out of an output from said first logical device and an output from said second logical device in response to a complementary clock signal to be used for outputting and to produce said first input data and to select an output out of an output from said third logical device and an output from said fourth logical device in response to a complementary clock signal to be used for outputting and to produce said second input data.

9. A slew rate controlling system for output data comprising:

a potential difference detecting circuit to detect a decrease in a potential difference among a first power supply and a second power supply to produce a first signal with specified timing and to detect an increase in a potential difference between said first power supply and said second power supply to produce a second signal with specified timing; and

a slew rate controlling circuit to exert, when said first signal is significant, control so as to enlarge a transition speed occurring at time of a fall of output data and, when said second signal is significant, so as to enlarge a transition speed occurring at time of a rise of output data to produce output data.

10. The slew rate controlling system for output data according to Claim 9, wherein said potential difference detecting circuit comprises a first differential amplification circuit to produce an output when a potential difference between said first power

supply and said second power supply becomes a preset value or less, a first sampling circuit to latch an output from said first differential amplification circuit with specified timing and to produce said first signal, a second differential amplification circuit to produce an output when a potential difference between said first power supply and said second power supply becomes said preset value or more, and a second sampling circuit to latch an output from said second differential amplification circuit and to produce said second signal.

11. The slew rate controlling system for output data according to Claim 9, wherein, in said potential difference detecting circuit, specified timing with which said first or second signal is produced is timing with which an external command is received.

12. The slew rate controlling system for output data according to Claim 11, wherein said external command is at least one of a writing command and a reading command in a memory device, an active command to provide an instruction for initiating operations of row systems, an MRS (Mode Register Set) command to provide an instruction for setting of an operating mode set register, and an EMRS (Extended Mode Register Set) command to provide an instruction for setting of an extended operating mode set register.

13. The slew rate controlling system according to Claim 9, wherein, in said potential difference detecting circuit, specified timing with which said first or second signal is produced is timing that is set at an another register when said

MRS command to provide an instruction for setting of an operating mode set register or said EMRS command to provide an instruction for setting of an extended operating mode set register is received.

14. The slew rate controlling system according to Claim 9, wherein said slew rate controlling circuit comprises a driver circuit to exert, when said first signal is significant, control on said first and second input data so as to enlarge a transition speed occurring at time of a fall of output data and, when said second signal is significant, so as to enlarge a transition speed occurring at time of a rise of output data and to produce first and second output data and an output buffer circuit to produce a high-level output when both said first and second output data are at a low level and to produce a low-level output when both said first and second output data are at a high level.

15. The slew rate controlling system according to Claim 14, wherein said slew rate controlling circuit comprises a logically-operated circuit having a first logical device to propagate and output a data signal to be output at time of a rise of an external clock when said output buffer is in an enable state and, when said output buffer is in a disenable state, its output is at a high level all the time, a second logical device to propagate and output a data signal to be output at time of a fall of an external clock when said output buffer is in an enable state and, when said output buffer is in a disenable state, its output is at a high level all the time, a third logical device to propagate and output a data signal to be output at time of a rise of an external clock when

said output buffer is in an enable state and, when said output buffer is in a disenable state, its output is at a low level all the time, and a fourth logical device to propagate and output a data signal to be output at time of a fall of an external clock when said output buffer is in an enable state and, when said output buffer is in a disenable state, its output is at a low level all the time and a selector circuit to select an output out of an output from said first logical device and an output from said second logical device in response to a complementary clock signal to be used for outputting and to produce said first input data and to select an output out of an output from said third logical device and an output from said fourth logical device in response to a complementary clock signal to be used for outputting and to produce said second input data.